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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,522	10/30/2003	Kazuyuki Suzuki	FUJI 20.710	8151

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EXAMINER	
AGA, SORI A	

ART UNIT	PAPER NUMBER
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,522	SUZUKI ET AL.	
	Examiner	Art Unit	
	Sori A. Aga	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/30/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim1and 2 rejected under 35 U.S.C. 103(a) as being unpatentable over Clauberg (EP 0 991 231) (herein after Clauberg) in view of Aramaki (US 6,982,975) (herein after Aramaki).

Regarding claim 1 where a packet processing apparatus is claimed, Clauberg teaches "a packet switch adaptor" (title).

Regarding the plurality of packet analyzing units for realizing parallel execution of information analyzing processes on the packets distributed from the distributor; Clauberg teaches "...When a distributor for distributing of the packets to several parallel, identical processing paths is used, ... packets can be distributed ...whereby a parallel processing is possible...".(Paragraph 0018 lines 1-6). Clauberg also teaches "...each comprising at least one processing unit, whereto the packets are fed and which is able to process only for one of the packets its packet information...." (Column 4 lines 7-11).

Regarding the order correction unit for receiving the packets, rearranging the packets in order according to the sequence number assigned to each of the packets and outputting the packets in the rearranged order; Clauberg teaches "...The substreams ...are fed into a multiplexer. This multiplexer is designed such that a

sequence of the packets, i.e. the chronological order on the input medium is reestablishable ..." (Column 9 line55 – Column 10 line 3).

However Clauberg does not explicitly teach a distributor for assigning a sequence number to each of a plurality of packets input to the distributor and distributing the packets, However Aramaki in the same field of endeavor as Clauberg (packet processing unit) teaches: "...unit switch (distributor) at the first stage assigns a sequence number to an input packet ...and distributes.... to a unit switch at a succeeding stage..." (Column 2 line 66 - column 3 line 2). Therefore it would have been obvious at the time of the invention to include a such a distributor in order to appropriately forward the packets to the following stage unit switches (packet analyzing units).

Claim 2: All the limitations of claim 1 are included in claim 2. Regarding the distributor distributing the packets to the packet analyzing units according to a value of a predetermined bit in each of the packets teaches "...when a selector for choosing packets from the priority queues is used...then a selection according to the priorities of the packets for further processing can be achieved..." (Column 3 lines 47-49). Therefore Clauberg teaches distributor that selects based on priority. Clauberg further teaches that " in general, the priority of a packet is any kind of information...stored in and delivered with the header of the packet..." (column 7 lines 8-11). Therefore, Clauberg teaches reading the header of a packet (predetermined bit) in order to determine priority and distribute among parallel processors.

3. Claim3 rejected under 35 U.S.C. 103(a) as being unpatentable over Clauberg and Aramaki as applied to claim 1 above and further in view of Yoshikawa (US 6,788,699) (herein after Yoshikawa).

Claim 3: All the limitations of claim 1 are included in claim 3. The references teach all the limitations of claim 1 as discussed above. However, Clauberg does not explicitly teach a distributor including a plurality of output buffers to which the packets are distributed. However Aramaki in the same field of endeavor teaches an output buffer in fig.3. Aramaki further teaches "...The packet stored in the output buffer is taken out in line with a speed of the output port and is output to the output port...". (Column 6 lines 57-60). It would have been obvious at the time of the invention for a person of ordinary skill in the art, to add an output buffer corresponding to each packet analyzing unit, in order to be able to take out packets from the buffer inline with the speed f the output port.

Regarding the distributor setting a threshold value to an amount of accumulated data in each of the output buffers and stop distributing the packets when the threshold is exceeded, Yoshikawa, in the same field of endeavor as Clauberg (packet processing apparatus) teaches "...when the number of cells staying in an output buffer exceeds this threshold value...temporarily stop sending cells addressed to ...output buffer ...By this, cells are prevented from being discarded in the output buffers ..." (column 2 lines 17-23). Therefore, it would have been obvious to set a threshold value to the amount of accumulated data in each of the output buffers and stop distributing the packets when the threshold is exceeded in order to prevent discarding of packets.

4. Claims 4 and 5 rejected under 35 U.S.C. 103(a) as being unpatentable over Clauberg and Aramaki as applied to claim 1 above and further in view of Rahim et al (US 7,085,274) (herein after Rahim).

Claim 4: All the limitations of claim 1 are included in claim 4. The references teach all the limitations of claim 1 as discussed above. However Clauberg does not explicitly teach an order correction unit including a packet buffer for storing the packets supplied from the packet-analyzing units, and an address manager having a plurality of entries corresponding to the sequence numbers assigned to the packets. However Rahim in the same field of endeavor (data processing) teaches a fabric communication component including a packet buffer. (figs,1 and 5 and Column 2 line 54-56).

Rahim teaches "...Spray block (buffer control unit) stores identification information 330, along with the corresponding data cell from data buffer..." (Column 5 lines 11-12). The 'identification information' includes entries corresponding to the sequence numbers assigned to the packets (column 5 lines 8-9). Therefore, storing identification information as thought by Rahim is considered the same as entering sequence numbers as claimed in the present application since Rahim teaches identification information includes sequence number.

Regarding the buffer control unit for storing packet buffer addresses; Rahim teaches "the cell identification information is also forwarded to reorder engine ...generates, for each packet, a packet order table ("POT") that references, in the

correct cell order, the cells in memory that comprise the packet..." (Column 5 lines 15-18).

Regarding the buffer control unit reading the packet buffer addresses from the entries of the address manager in order according to the sequence number and outputting them in the read order; the invention Rahim enclosed is used to reorder and transmit packets. Reorder and transmit is considered to be substantially the same as reorder and output.

Therefore, it would have been obvious at the time of the invention to include a buffer control unit for storing packet information corresponding buffer addresses with sequence number and reading out the packets from the buffer in order according to the sequence number in as disclosed by Rahim in order to re-sequence the packets in the same order as they entered through the input of the device.

Claim 5: All the limitations of claim 4 are included in claim 5 except that the packet buffer addresses are read after the packet addresses have been stored in all the entries of the address manager. Clauberg does not explicitly teach that the packet buffer addresses are read after the packet addresses have been stored in all the entries of the address manager . However Rahim teaches that identification information is entered and the identification information includes both sequence number packet buffer address. Therefore, Rahim teaches that packet addresses and entries of the address manager (i.e. sequence numbers) are entered before transmission is done. Sequence number includes both information on both sequence numbers buffer addresses as discussed above regarding claim 4 above.

Therefore, it would have been obvious at the time of the invention to enter identification information both sequence number and buffer addresses to reduce the number of separate processes of entering packet information by entering both information at once for each packet stored.

5. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Clauberg, Aramaki and Rahim as applied to claim 5 above and further in view of Kobayahi et al (US 4,825,436) (herein after Kobayashi).

Claim 6: All the limitations of claim 5 are included in claim 6. The references teach all the limitations of claim 5 as discussed above. However, Clauberg does not explicitly teach an order correction unit including a first dysfunction detector for detecting a dysfunction when a difference between the number of packets stored in the packet buffer and the number of packets read from the packet buffer exceeds a predetermined value; However, Kobayashi in the same field of endeavor (packet processing) teaches "...In the system of the present invention, the write-in frame and read-out frame of a buffer memory are inspected ...."(column 2 lines 3-5). Kobayashi also teaches "...when the difference between the write-in frame and the read-out frame returns to β frames or larger, the frequency of the read-out clock signal is returned to the original value ...thereby regenerating the original data before the time division multiplexing...."(column 2 lines). Therefore it would have been obvious at the time of the invention for a person having ordinary skill in the art, to include a detector for detecting the difference between the number of packets stored and number of packets read form

the buffer exceeds a predetermined value (β) in order to be able to decide when to regenerate original data.

6. Claim7 rejected under 35 U.S.C. 103(a) as being unpatentable over Clauberg, Aramaki and Rahim as applied to claim 4 above and further in view of Ziegler et al (US 2003/0112798) (herein after Ziegler).

Claim 7: All the limitations of claim 4 are included in claim 7. The references teach all the limitations of claim 4 as discussed above. However, Clauberg does not explicitly teach a dysfunction detector for detecting when the entry corresponding to buffer address where packet buffer address has just been stored is ahead of the entry from which the packet buffer address is to be read by more than a window value. However Ziegler in the same field of endeavor as Clauberg teaches a fullness indicator i.e. distance between the write pointer and the read pointer (Paragraph 0024 lines 9-11). This distance is considered to be considerably the same as the distance between the entry of the address manager in which the packet buffer address has best been stored (as in the present application) and the entry from which the packet buffer address is to be read. A person having ordinary skill in the art would know write pointer points to the address where the last packet was just entered right before the write pointer is incremented to point to the next available position to write. Similarly, the read pointer keeps track of the next position to be read and therefore points to the last memory read immediately after the packet is read and right before its value is altered to point to the next position to be read. Ziegler also refers to this difference

between write pointer and read pointer 'fullness of FIFO'. (paragraph 0024 line 14).

Ziegler teaches "...The system needs to respond appropriately when the FIFO fullness is greater than a first predetermined threshold, or in other words when the FIFO is getting too close to being full...". Therefore it would have been obvious at the time of the invention to include a dysfunction detector to detect memory fullness that is greater than a threshold value in order to prevent new data from being written over a memory where the old data has not been read yet.

7. Claim8 rejected under 35 U.S.C. 103(a) as being unpatentable over Clauberg, Aramaki, Rahim and Ziegler as applied to claim 7 above and further in view of Olnowich (US 5,612,953) (herein after Olnowich).

Claim 8: All the limitations of claim 7 are included in claim 8. all the limitations of claim 7 are thought by the references as discussed above regarding claim 7. However Clauberg does not explicitly teach an order correction that resumes reading the packet buffer addresses from the address manager starting from the earliest entry of the unbroken succession. However, Olnowich in the same field of endeavor (network device) teaches "...Block 180 can retry the transmission of a message or partial message to network 30 from buffer by issuing the RETRY signal, which rolls back the value of read counter 258 by setting read counter 258 equal to the read pointer, pointing it back to the beginning of the valid message so that it can be reread..." (Column 36 lines 41-46). Therefore, it would have been obvious for a person having ordinary skill in the art to make Clauberg's device to

rolling back the read counter to the beginning to the valid message (earliest entry of unbroken succession) in order to recover (retransmit) missing packets.

8. Claim9,10 and 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Clauberg and Aramaki as applied to claim 1 above and further in view of Ganesh et al (US 6,553,000) (herein after Ganesh).

Claim 9 and 11: All the limitations of claim 1 are included in clam 9 and 11. The references teach all the limitations of claim 1 as discussed regarding cliam1. However, Clauberg does not teach a search means for integrally performing search processes using an associative memory. However, Ganesh in the same field of endeavor (packet processing apparatus) teaches that a search engine coupled with a CAM memory can be used in a switching device as shown in figure 2 (and described in column 4 lines 31-33) and (Column 8 line 55-56). Fig. 2 shows search engine 48 integrated within the switching device 40. Therefore, it would have been obvious at the time of the invention to integrate a search engine that executes search using associative memory (CAM) in the device thought by Clauberg at the time of the invention in order to find network addresses saved in a lookup table when needed.

Claim 10: all the limitations of claim 9 are included in claim 10. The references teach all the limitations of claim 9 as discussed above.

Regarding the search engine having the function of mediating accesses, Ganesh teaches that an arbitration device can be used to grant accesses (column 4 lines 59-61). Therefore, it would have been obvious at the time of the invention for a

person having ordinary skill in the art to include a arbitration device in order to facilitate access to the search engine in a fairly among processing units.

9. Claim 12 rejected under 35 U.S.C. 103(a) as being unpatentable over Clauberg, Aramaki and Ganesh as applied to claim 11 above and further in view of Murase (US 6, 993,031) (herein after Murase).

Claim 12: all the limitations of claim 11 are included in claim 12. The references teach all the limitations of claim 11 as discussed above.

However, Clauberg does not explicitly teach a search means arranged to calculate a number of hits made for each of entries provided in the associative memory.

However Murase in the same field of endeavor (packet processing device) teaches writing a hit record table including information on the number of hits (column 6 lines 2 and 30). The number of hits information is used to make up a priority list.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sori A. Aga whose telephone number is (571) 270-1868. The examiner can normally be reached on M-Th 7:30-5:00, F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 270-1868. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

S.A.